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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/505,433 | 08/24/2004 | Hiroshi Iwata | 0020-5288PUS1 | 3663 |

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| EXAMINER | |
|---|---|
| DICKEY, THOMAS L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

5K

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/505,433 | IWATA ET AL. | |
| | Examiner | Art Unit | |
| | Thomas L. Dickey | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/24/04 & 7/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

**1.** The preliminary amendment filed on 08/24/04 has been entered.

### *Oath/Declaration*

**2.** The oath/declaration filed on 08/24/04 is acceptable.

### *Drawings*

**3.** Figure 21 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Priority*

**4.** Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

**5.** The Information Disclosure Statements filed on August 24 2004 and July 7 2005 have been considered.

### *Specification*

**6.** The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Double Patenting*

**7.** The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obvious-ness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by (as is the case here), or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-5 and 9-13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 8-1 of copending Application No. 10/506322. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1 and 8-13 of 10/506322 disclose each and every limitation of Claims 1-5 and 9-13 of the instant application. The claims avoid a statutory double patenting rejection only because the channel claimed in claim 1 or the copending application may meet that claim by being formed in either a substrate, a well region, or an SOI region (note claim 1 lines 2-5 of copending Application No. 10/506322), whereas to meet claim 1 of the instant application the channel must be formed in a substrate (no substitutions allowed).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 102***

**8.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**A.** Claims 1-5,8, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by YOSHIKAWA (4,881,108).

Yoshikawa discloses a semiconductor storage device comprising a semiconductor substrate 101; a gate insulating film 103 formed on the semiconductor substrate 101; a single gate electrode 104 formed on the gate insulating film 103; two charge holding portions 108 formed on the sidewalls on opposite sides of the single gate electrode 104; two diffusion layer region 112-113 corresponding to the two charge holding portions 108 respectively; and, a channel region (note column 1 lines 26-28) placed beneath the single gate electrode 104, wherein the charge holding portions 108 have a structure

such that a first film insulator 106 having a function of holding charge is sandwiched between a second film insulator 105 separating the semiconductor substrate 101 and the sidewalls of the gate electrode 104 from the first film insulator 106 and a third film insulator 107, and the charge holding portions 108 are constituted such that the amount of current flowing between one of the diffusion layer region 112-113 and the other of the diffusion layer region 112-113 at the time of application of a voltage to the gate electrode 104 is changed due to the quantity of charge held in the first film insulator 106, and that the first film insulator 106 is of silicon nitride, and the second film insulator 105 and third film insulator 107 are of silicon oxide, so that all expressions (noting that applicant admits at paragraphs 40 and 87 of the instant application that all of these expressions are satisfied when the first film insulator 106 is of silicon nitride, and the second film insulator 105 and third film insulator 107 are of silicon oxide) of: $X1 > X2$, $X1 > X3$, $\Phi 1 > \Phi 2$ and $\Phi > \Phi 3$ are satisfied, where the X1 represents an energy gap between the vacuum level and the lowest level of the conduction band of the first film insulator 106, the X2 represents an energy gap between the vacuum level and the lowest level of the conduction band of the second film insulator 105, the X3 represents an energy gap between the vacuum level and the lowest level of the conduction band of the third film insulator 107, the $\Phi 1$ represents an energy gap between the vacuum level and the highest level of the valence band of the first film insulator 106, the $\Phi 2$ represents an energy gap between the vacuum level and the highest level of the

valence band of the second film insulator 105, and the Φ3 represents an energy gap between the vacuum level and the highest level of the valence band of the third film insulator 107,that the second film insulator thickness in the vicinity of the sidewalls of the gate electrode 104 is greater than the second film insulator thickness on the semiconductor substrate 101, and that the first film insulator 106 includes a portion that extends approximately parallel to sides of the gate electrode 104. Note figure 1a-c and column 4 lines 8-65 of Yoshikawa.

**B.** Claims 1-8 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by SAKAGAMI ET AL. (5,838,041).

Sakagami et al. discloses a semiconductor storage device comprising a semiconductor substrate 1; a gate insulating film 11 formed on the semiconductor substrate 1; a single gate electrode 13 formed on the gate insulating film 11; two charge holding portions 19 formed on the sidewalls on opposite sides of the single gate electrode 13; two diffusion layer regions 20,21 corresponding to the two charge holding portions 19 respectively; and, a channel region (marked as part #8 in prior art figure 1, but part of the disclosed invention) placed beneath the single gate electrode 13, wherein the charge holding portions 19 have a structure such that a first insulator film 17, including a portion that extends approximately parallel to sides of the gate electrode 13, having a function of holding charge is sandwiched between a second insulator film 14 separating the semiconductor substrate 1 and the sidewalls of the gate electrode 13 from the first insulator film 17, and a third insulator film 18, and the charge holding

portions 19 are constituted such that the amount of current flowing between one of the diffusion layer regions 20,21 and the other of the diffusion layer regions 20,21 at the time of application of a voltage to the gate electrode 13 is changed due to the quantity of charge held in the first insulator film 17, that the first insulator film 17 is of silicon nitride, and the second insulator film 14 and third insulator film 18 are of silicon oxide, so that all expressions (noting that applicant admits at paragraphs 40 and 87 of the instant application that all of these expressions are satisfied when the first insulator film is of silicon nitride, and the second insulator film and third insulator film are of silicon oxide) of: $X1 > X2$, $X1 > X3$, $\Phi 1 > \Phi 2$ and $\Phi > \Phi 3$ are satisfied, where the X1 represents an energy gap between the vacuum level and the lowest level of the conduction band of the first insulator film 17, the X2 represents an energy gap between the vacuum level and the lowest level of the conduction band of the second insulator film 14, the X3 represents an energy gap between the vacuum level and the lowest level of the conduction band of the third insulator film 18, the $\Phi 1$ represents an energy gap between the vacuum level and the highest level of the valence band of the first insulator film 17, the $\Phi 2$ represents an energy gap between the vacuum level and the highest level of the valence band of the second insulator film 14, and the $\Phi 3$ represents an energy gap between the vacuum level and the highest level of the valence band of the third insulator film 18, wherein the thickness of the film made of the second insulator film 14 in the vicinity of the sidewalls of the gate electrode 13 is greater than the thickness of

the film made of the second insulator film 14 on the semiconductor substrate 1; at least a portion of the first insulator film 17 overlaps a portion of the diffusion layer regions 20,21; the first insulator film 17 includes a portion having a surface approximately parallel to the surface of the gate insulating film 11, the second insulator-film thickness (being 2-10 nm, note column 4 line 64 and column 5 line 1) is no less than 1.5 nm and no greater than 15 nm, and the first insulator-film thickness (being 0.5-7 nm, note column 5 lines 22-26) is no less than 2 nm and no greater than 15 nm. Note figures 2, 7, column 4 lines 6-35, and column 5 lines 30-35 of Sakagami et al.

**C.** Claims 1-7 and 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by YOSHIKAWA (6,335,554).

Yoshikawa discloses a semiconductor storage device comprising a semiconductor substrate 1; a gate insulating film 2, having a gate insulating film thickness (2-25 nm, note column 7 line 36), formed on the semiconductor substrate 1; a single gate electrode 3 formed on the gate insulating film 2; two charge holding portions 4a-b formed on the sidewalls on opposite sides of the single gate electrode 3; two diffusion layer regions 10 corresponding to the two charge holding portions 4a-b respectively; and a channel region placed beneath the single gate electrode 3, wherein the charge holding portions 4a-b have a structure such that a first insulator film 6, having a first insulator film thickness (10-100 nm, note column 7 line 51) including a portion that extends approximately parallel to sides of the gate electrode 3, having a function of holding charge is sandwiched between a second insulator film 5, having a second

insulator film thickness (10 nm, note column 7 line 49), separating the semiconductor substrate 1 and the sidewalls of the gate electrode 3 from the first insulator film 6, and a third insulator film 7, and the charge holding portions 4a-b are constituted such that the amount of current flowing between one of the diffusion layer regions 10 and the other of the diffusion layer regions 10 at the time of application of a voltage to the gate electrode 3 is changed due to the quantity of charge held in the first insulator film 6, that the first insulator film 6 is of silicon nitride, and the second insulator film 5 and third insulator film 7 are of silicon oxide, so that all expressions (noting that applicant admits at paragraphs 40 and 87 of the instant application that all of these expressions are satisfied when the first insulator film is of silicon nitride, and the second insulator film and third insulator film are of silicon oxide) of: $X1 > X2$, $X1 > X3$, $\Phi 1 > \Phi 2$ and $\Phi > \Phi 3$ are satisfied, where the X1 represents an energy gap between the vacuum level and the lowest level of the conduction band of the first insulator film 6, the X2 represents an energy gap between the vacuum level and the lowest level of the conduction band of the second insulator film 5, the X3 represents an energy gap between the vacuum level and the lowest level of the conduction band of the third insulator film 7, the $\Phi 1$ represents an energy gap between the vacuum level and the highest level of the valence band of the first insulator film 6, the $\Phi 2$ represents an energy gap between the vacuum level and the highest level of the valence band of the second insulator film 5, and the $\Phi 3$ represents an energy gap between the vacuum level and the highest level of the

valence band of the third insulator film 7, wherein the second insulator film thickness in the vicinity of the sidewalls of the gate electrode 3 is greater than the second insulator film thickness on the semiconductor substrate 1, at least a portion of the first insulator film 6 overlaps a portion of the diffusion layer regions 10, the first insulator film 6 further includes a portion having a surface approximately parallel to the surface of the gate insulating film 2, the second insulator film thickness (10 nm, note column 7 line 49) is no less than 1.5 nm and no greater than 15 nm, the first insulator film thickness (10-100 nm, note column 7 line 51) is no less than 2 nm and no greater than 15 nm, and the second insulator film thickness (10 nm, note column 7 line 49) may be less than the gate insulating film thickness (2-25 nm, note column 7 line 36) and not less than 0.8 nm, and may be greater than the gate insulating film thickness (2-25 nm, note column 7 line 36) not greater than 20 nm. Note figure 6, column 6 lines 22-36, and column 7 lines 40-55 of Yoshikawa.

**D.** Claims 1-10,12, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by KOBAYASHI ET AL. (2003/0161192).

Kobayashi et al. discloses a semiconductor storage device comprising a semiconductor substrate 1; a gate insulating film 4, having a gate insulating film thickness (1-10 nm, note paragraph 0103), formed on the semiconductor substrate 1; a single gate electrode 5 formed on the gate insulating film 4; two charge holding portions 6a-6b formed on the sidewalls on opposite sides of the single gate electrode 5; two diffusion layer regions 2a-2b corresponding to the two charge holding portions 6a-6b

respectively; and a channel region Ch2 placed beneath the single gate electrode 5, wherein the charge holding portions 6a-6b have a structure such that a first insulator film 6-2, having a first insulator film thickness (3.5-6.0 nm, note paragraph 0108), including a portion that extends approximately parallel to sides of the gate electrode 5, having a function of holding charge is sandwiched between a second insulator film 6-1, having a second insulator film thickness (2.5-6.0 nm, note paragraph 0107), separating the semiconductor substrate 1 and the sidewalls of the gate electrode 5 from the first insulator film 6-2, and a third insulator film 6-3, and the charge holding portions 6a-6b are constituted such that the amount of current flowing between one of the diffusion layer regions 2a-2b and the other of the diffusion layer regions 2a-2b at the time of application of a voltage to the gate electrode 5 is changed due to the quantity of charge held in the first insulator film 6-2, that the first insulator film 6-2 is of silicon nitride, and the second insulator film 6-1 and third insulator film 6-3 are of silicon oxide, so that all expressions (noting that applicant admits at paragraphs 40 and 87 of the instant application that all of these expressions are satisfied when the first insulator film is of silicon nitride, and the second insulator film and third insulator film are of silicon oxide) of: $X1 > X2$, $X1 > X3$, $\Phi 1 > \Phi 2$ and $\Phi > \Phi 3$ are satisfied, where the X1 represents an energy gap between the vacuum level and the lowest level of the conduction band of the first insulator film 6-2, the X2 represents an energy gap between the vacuum level and the lowest level of the conduction band of the second insulator film 6-1, the X3 represents an energy gap between the vacuum level and the lowest level of the

conduction band of the third insulator film 6-3, the $\Phi 1$ represents an energy gap between the vacuum level and the highest level of the valence band of the first insulator film 6-2, the $\Phi 2$ represents an energy gap between the vacuum level and the highest level of the valence band of the second insulator film 6-1, and the $\Phi 3$ represents an energy gap between the vacuum level and the highest level of the valence band of the third insulator film 6-3, wherein the thickness of the film made of the second insulator film 6-1 in the vicinity of the sidewalls of the gate electrode 5 is greater than the thickness of the film made of the second insulator film 6-1 on the semiconductor substrate 1, the first insulator film 6-2 includes a portion having a surface approximately parallel to the surface of the gate insulating film 4, the second insulator film thickness (2.5-6.0 nm, note paragraph 0107) is no less than 1.5 nm and no greater than 15 nm, the first insulator film thickness (3.5-6.0 nm, note paragraph 0108) is no less than 2 nm and no greater than 15 nm, the second insulator film thickness (2.5-6.0 nm, note paragraph 0107) is less than the gate insulating film thickness (1-10 nm, note paragraph 0103) and not less than 0.8 nm, and the second insulator film thickness (2.5-6.0 nm, note paragraph 0107) is greater than the gate insulating film thickness (1-10 nm, note paragraph 0103) not greater than 20 nm. Note figures 1A, 1B, and paragraphs 0099-0111 of Kobayashi et al.

***Conclusion***

**9.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Thomas L. Dickey**
**Patent Examiner**
**Art Unit 2826**
**02/06**